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A magnetic-linked multilevel active neutral point clamped converter with an advanced switching technique for grid integration of solar photovoltaic systems

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Abstract

© 1972-2012 IEEE. Nowadays, the grid-connected solar photovoltaic (PV) system has been drawing significant attention due to the rapid development and the decreasing cost of solar panels. The efficiency and reliability of a grid-connected PV system mainly depend on the power conversion system and the control strategy. This article presents a new magnetic-linked 7-level active neutral point clamped (ANPC) converter, which requires less number of flying capacitors and also reduces the control complexity of the grid-connected PV system. The proposed converter topology utilizes the input dc bus voltage better than the traditional ANPC multilevel converter and also provides galvanic isolation to the grid-connected PV systems. The lack of galvanic isolation is one of the biggest problems faced by the power frequency transformerless grid-connected PV systems. The proposed magnetic-linked power converter is also validated through simulations in MATLAB/Simulink and through tests in a laboratory test platform.

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A Magnetic linked Multilevel Active Neutral Point Clamped Converter with an Advanced Switching Technique for Grid Integration of Solar Photovoltaic Systems

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***Abstract*— Nowadays, the grid connected solar photovoltaic (PV) system has been drawing significant attention due to the rapid development and the decreasing cost of the solar panels. The efficiency and the reliability of a grid connected PV system mainly depend on the power conversion system and the control strategy. This paper presents a new magnetic linked 7-level active neutral point clamped (ANPC) converter, which requires less number of flying capacitors and also reduces the control complexity of the grid connected PV system. The proposed converter topology utilizes the input dc bus voltage better than the traditional ANPC multilevel converter and also provides galvanic isolation to the grid connected PV systems. The lack of galvanic isolation is one of the biggest problems faced by the power frequency transformer-less grid connected PV systems. The proposed magnetic linked power converter is also validated through simulations in MATLAB/Simulink and through tests in a laboratory test platform.**

***Keywords*—Solar photovoltaic, grid integration, power converter topology, modulation technique, power losses.**

I. Introduction

POWER electronics systems play an important role in distributed power generation and in the interconnection between the grid and the renewable energy sources, such as solar photovoltaic (PV) systems [1]–[5]. Due to the rapid expansion of the PV power plant market, more emphasis has been placed on the PV power converter topologies. The multilevel converters are becoming the preferred choice for use in the grid integration of the solar PV systems, due to their improved output power quality and the high voltage handling capability [1]–[5]. There are three basic types of the multilevel inverter, the cascaded H-bridge (CHB), the flying capacitor (FC) and the neutral point clamp (NPC) multilevel inverter [6]–[8]. With the increase of the number of voltage levels, the number of the isolated transformers, the flying capacitors and the clamping diodes, increases tremendously for the CHB, FC and NPC respectively. Moreover, for the traditional basic multilevel inverters, the control system becomes more complex with the increase of the numbers of the voltage levels [9], [10].

Nowadays, the stacked multi-cell converter (SMC) [11], the modular multilevel converter (MMC) [3], [12], and the active neutral point clamped (ANPC) [13] are the emerging multilevel inverters. In MMC, cascaded half bridges are used to provide the high voltage output. But in the MMC, the floating capacitors can experience low frequency fluctuations [14]. The SMC, where several FC converters are stacked together, suffers from the same problems faced by the FC multilevel inverter. The ANPC is the multilevel converter that can eliminate some of the problems faced by the CHB, FC, NPC, MMC and SMC. The ANPC requires less number of clamping devices and flying capacitors compared with the MMC, NPC, FC and SMC. But the ANPC suffers from the reduced dc bus utilization issue and also requires a complex control strategy to balance the flying capacitor voltages.

In this paper, a new 7-level ANPC magnetic linked power converter is proposed, which improves the dc bus voltage utilization compared with that of the traditional ANPC and solves the capacitor voltage balancing issues using a high frequency magnetic link. The proposed converter topology requires less number of flying capacitors, which makes the power conditioning system compact and more reliable. An advanced pulse width modulation (PWM) technique is also investigated with the proposed magnetic linked power converter to improve the efficiency of the power conditioning system. For comparison, the performance of the traditional PWM techniques with the proposed power converter topology is also presented in this paper. The suitability of the proposed converter and control strategy is validated both through simulations and tests in a laboratory test platform.

The main contributions of this paper are:

- The paper proposes a new power converter topology;
- The proposed converter has reduced number of capacitors;
- The proposed converter has a better utilization of the dc bus voltage;

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- The proposed converter can solve the capacitor voltage balancing issue with the use of the proposed high frequency magnetic link.

II. Proposed Magnetic Linked Converter

In this paper, a 7-level magnetic linked ANPC inverter is proposed which requires the same number of electronic switches as the traditional ANPC 7-level inverter, but the proposed topology requires less number of flying capacitors compared to the traditional ANPC inverter. It is worth to mention that, the traditional ANPC requires 2 flying capacitors to obtain a 7-level inverter, whereas, the proposed topology requires only one flying capacitor to obtain a 7-level inverter. The main problems with the traditional ANPC inverter are (i) only a maximum of 50% of the input dc bus voltage can be utilized and (ii) a strategy is required to balance the flying capacitor voltages. The proposed ANPC can utilize 75% of the input dc bus voltage and can also eliminate the voltage balancing problems faced by the traditional ANPC inverters.

Fig. 1 shows the proposed magnetic linked power converter topology for the grid integration of the PV systems. In this paper, the high frequency magnetic link has been used to ensure that for each single phase, the output voltage of the top rectifier is always 4 times the output voltage of the bottom rectifier by using different winding turns between the input winding of the top rectifier (4N) and the input winding of the bottom rectifier (N).

First, the dc power from the PV array is converted into a high frequency ac and then fed into the high frequency magnetic link. Two secondary windings are used to produce two dc voltages for each single phase unit. One winding is used to supply the dc-link capacitors (C_1 and C_2) and the other winding is used to supply the flying capacitor (C_{fc}). In Fig. 1, the output voltage of the top rectifier (across the two dc link capacitors (C_1 and C_2)) is 4 times the output voltage of the bottom rectifier (across the flying capacitor (C_{fc})), therefore if the voltage across the two dc link capacitors (C_1 and C_2) of each single phase unit is defined as V_{dc} (the voltage across C_1 or C_2 is $V_{dc}/2$) then the voltage across the flying capacitor (C_{fc}) is $V_{dc}/4$. The ratio of the dc-link capacitor voltage to the flying capacitor winding is therefore always maintained at 4. Finally, the dc voltages are fed into the 7-level ANPC to obtain the seven different voltage levels as shown in Table I.

TABLE I
SWITCHING TABLE

State	Switching states										V_{out}
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	
1	off	on	on	off	on	off	off	off	off	off	$V_{dc}/4$
2	on	off	on	off	on	off	off	off	off	off	$V_{dc}/2$
3	on	off	off	off	on	on	off	off	off	off	$3V_{dc}/4$
4	on	off	off	on	off	off	off	on	off	off	$-V_{dc}/4$
5	off	on	off	on	off	off	off	on	off	off	$-V_{dc}/2$
6	off	on	off	off	off	off	on	on	off	off	$-3V_{dc}/4$
7a	on	off	off	off	off	off	off	off	on	off	0
7b	on	off	off	off	off	off	off	off	off	on	0

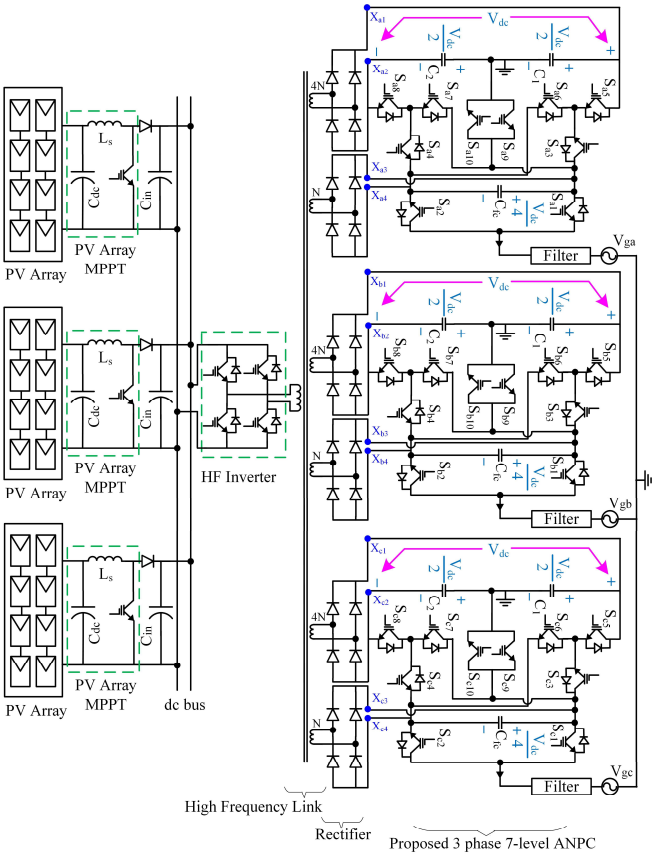

Fig. 1. The proposed 7-level ANPC magnetic linked inverter for grid integration of PV systems.

Fig. 2 shows the first four modes of operation for the proposed power converter topology.

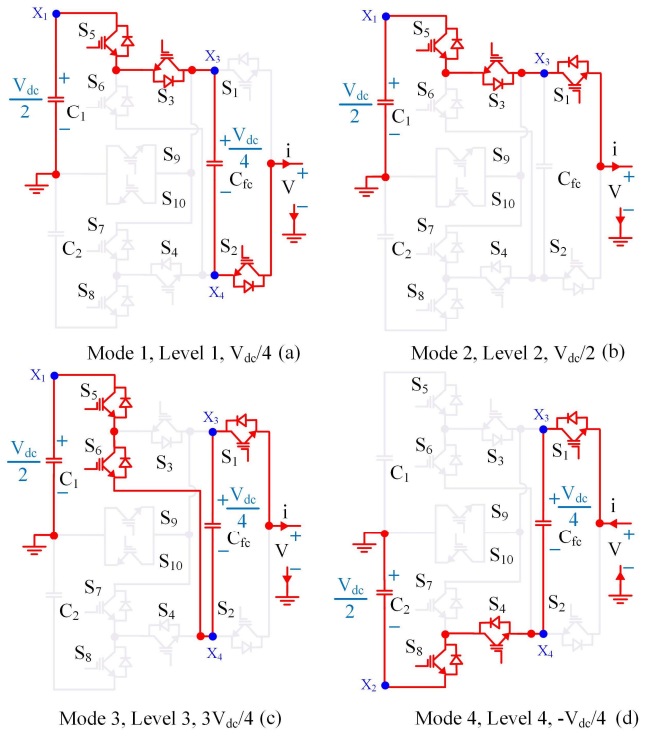

Fig. 2. First four modes for the proposed power converter.

Fig. 2(a) shows the mode 1 operation, where the output voltage is given by $V_{dc}/2 - V_{dc}/4 = V_{dc}/4$. Although there is a voltage across C_2, it is inactive due to the switching states. Similarly, Fig. 2(b) shows the mode 2 operation, where the output voltage is given by $V_{dc}/2$. Fig. 2(c) shows the mode 3 operation, where the output voltage is given by $V_{dc}/2 + V_{dc}/4 = 3V_{dc}/4$. The remaining Fig. 2(d) is self-explanatory.

Fig. 3 shows the last four modes of the power converter and can be explained in the same way as Fig. 2. The voltage stress for S_5 and S_8 is V_{dc} and the voltage stress for S_1, S_2, S_3, S_4, S_6 and S_7 is $V_{dc}/4$. The S_9 and the S_{10} are used to obtain a proper zero state of the inverter. The voltages across these switches are $3V_{dc}/4$.

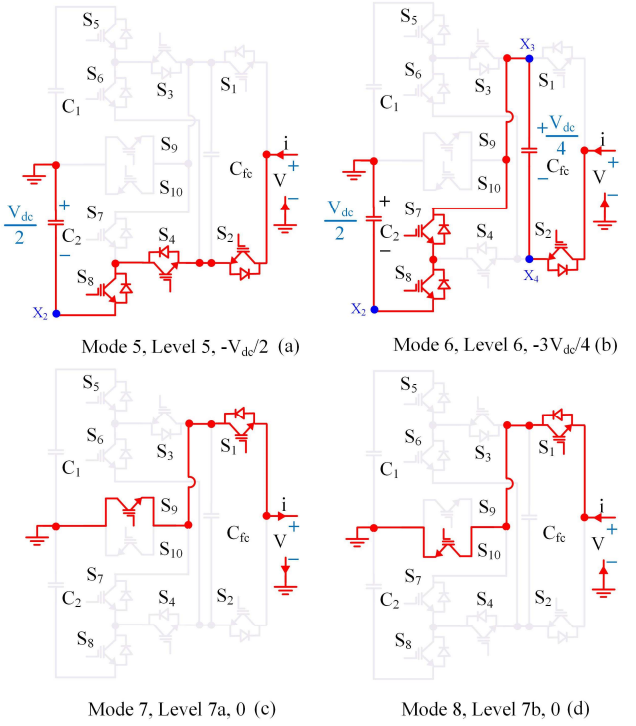

Fig. 3. Last four modes for the proposed power converter.

Fig. 4(a) shows the amorphous ribbon (20 µm thick and 2.5 cm wide), Fig. 4(b) shows the preparation of the magnetic core and Fig. 4(c) shows the prepared magnetic core for the proposed ANPC converter topology. The amorphous ribbon is placed in the circular structure of the core development platform and araldite glue has been used for metallic bonding and for maintaining no air gap in the core. The number of turns of the windings is different from each other as shown in Fig. 4(c). For the validation of the proposed power converter topology, 7 windings are used. One winding is the primary winding and the remaining windings are used as secondary windings. The amorphous materials Metglas alloys 2605S3A and 2605SA1 are manufactured by Hitachi Metals Ltd. The saturation flux density of the Metglas alloy 2605S3A is 1.4 T. The core loss in terms of the flux density and the frequency is shown in Fig. 4 (d). At 0.5 T flux density, with a square wave excitation and a 10 kHz frequency, the core loss is 100 W/kg.

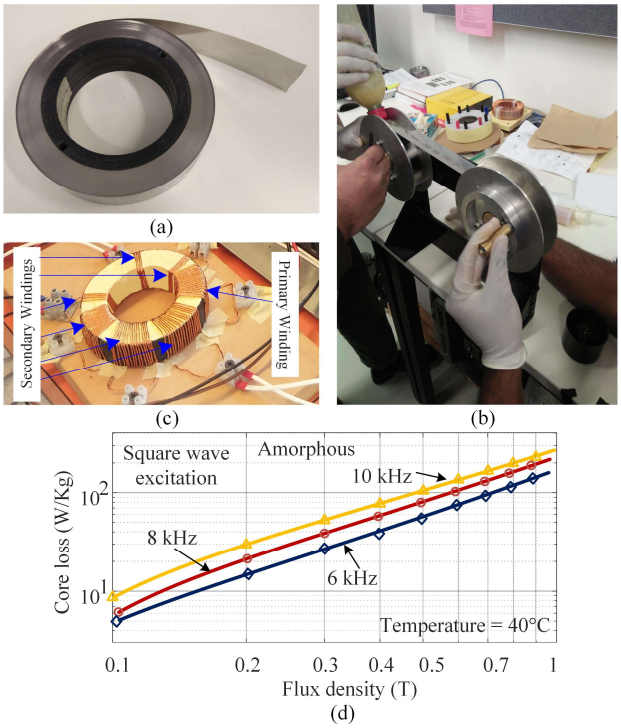

Fig. 4. (a) Amorphous ribbon, (b) preparation of the magnetic core, (c) prepared magnetic core, and (d) core loss in terms of flux density and frequency.

Fig. 5 shows the control scheme for the proposed power converter topology. At first the reference direct axis component (I_d*) is obtained from the dc link voltage regulator and the reference quadrature axis component (I_q*) is set to zero due to the operation of the inverter at unity power factor. Then the error between the actual grid injected currents (I_d and I_q) and the reference currents (I_d* and I_q*) are passed through the PI controllers and eventually the direct axis component of the inverter reference voltage (V_d*) and the quadrature axis component of the inverter reference voltage (V_q*) are calculated. Finally, the direct and quadrature axis component of the reference inverter voltage are converted into the three phase reference voltages, which are then compared with the high frequency carrier waves to generate the pulses for the electronic switches for the proposed ANPC converter topology.

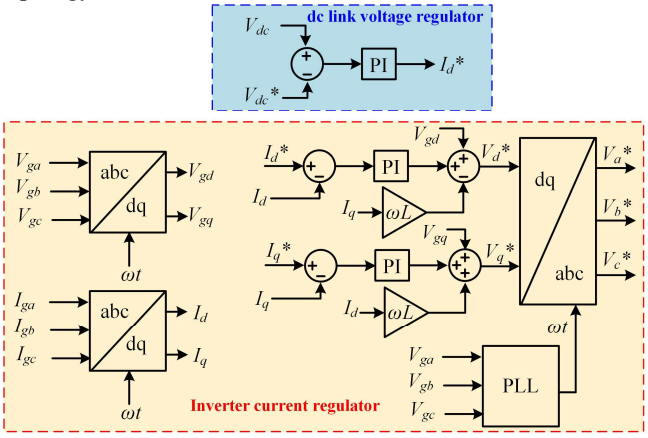

Fig. 5. The control scheme for the proposed power converter.

Fig. 6 shows the gate pulses for the proposed ANPC converter topology. The S_9 and the S_{10} switches are in operation while obtaining the zero state of the voltage. Therefore, these switches are in less operation compared to those of the other switching devices. The S_5 and S_8 switches remain in more conduction compared to the other switches. Therefore, these switches experience more conduction loss than the other switches. The switching and conduction loss distribution among the electronic switches have been discussed in the loss analysis section of this paper.

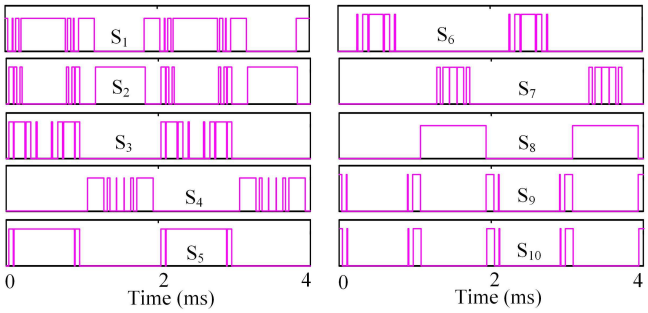

Fig. 6. Gate pulses for the proposed ANPC converter topology.

Fig. 7 shows the simulation results for the proposed power converter topology with carrier frequency of 1 kHz. The output line voltage of the proposed converter and the frequency spectrum of the line voltage are shown in Fig. 7(a) and 7(b). Fig. 7(c) and Fig. 7(d) show the voltages across the capacitors C_1, C_{fc} and C_2. Fig. 7(e) shows the injected power to the grid by the PV arrays. Fig. 7(f) shows the phase voltage and the phase current of the grid while receiving power from the PV array. The simulation results show the voltages across the capacitors are almost constant over time. Table II shows the values of the different parameters used for the simulation.

TABLE II
SIMULATION PARAMETER

Parameter	Value
PV array	1.5 kW
Grid voltage	400 V (L-L)
Grid frequency	50 Hz
Carrier wave	Level shifted [15], 1 kHz
dc link capacitors	100 µF
Flying capacitor	100 µF
Filter inductor (L)	1 mH

Fig. 8 shows the inverter responses when there are fluctuations in the grid, such as the grid voltage sag and swell phenomenon. When there is a voltage sag or swell at the grid side, the voltage is sensed by the inverter. Due to the change in voltage amplitude the value of V_{gd} (direct axis component of grid voltage) *and* V_{gq} (quadrature axis component of grid voltage) are also changed and the inverter changes the modulation index accordingly.

When voltage sags occur, the inverter reduces its modulation index, and when voltage swells occur, the inverter increases its modulation index to cope with the grid voltage. Therefore, the inverter always tracks the grid voltage and changes the injected current to the grid according to the available PV power.

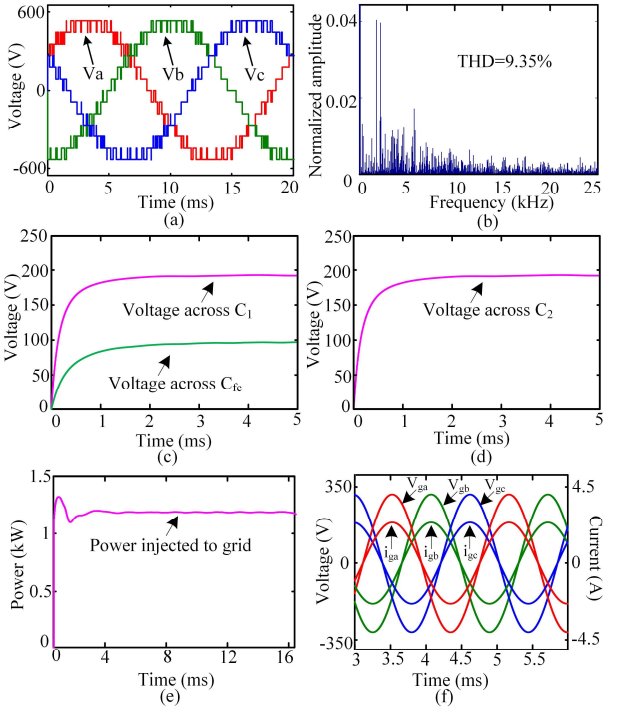

Fig. 7. (a) The output line voltage of the proposed ANPC inverter, (b) frequency spectrum of the output voltage, (c) voltage across the C_1 and C_{fc} capacitor, (d) voltage across the C_2 capacitor, (e) power injected to the grid, and (f) phase voltage and phase current of the grid.

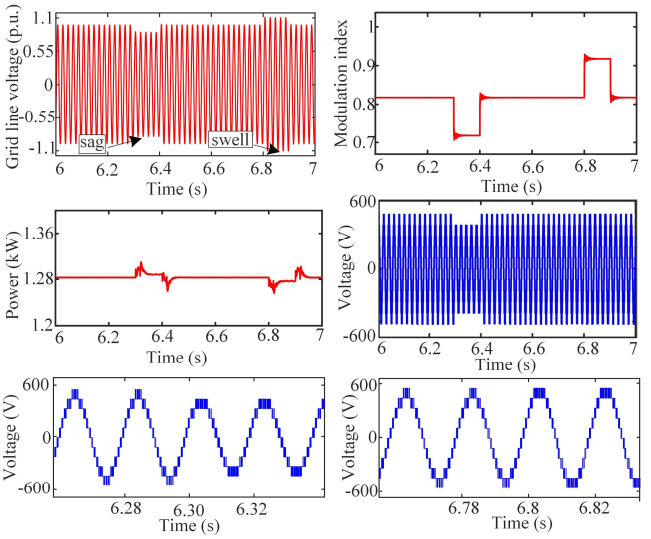

Fig. 8. System response when the grid side faces some vibration (a) grid side voltage, (b) modulation index of the inverter, (c) power injected to grid, (d) inverter line voltage, (e) zoomed inverter line voltage during sag, and (f) zoomed inverter line voltage during swell.

Fig. 9 shows the power imbalance analysis for the proposed power converter topology. When all the PV arrays experience the same insolation of 1 kW/m^2, then the current injected to the grid is obtained as 2.17 A rms. On the other hand, when the PV arrays experience different insolation like 1 kW/m^2,

0.75 kW/m^2, and 0.5 kW/m^2, then the injected current to the grid is obtained as 1.6 A rms.

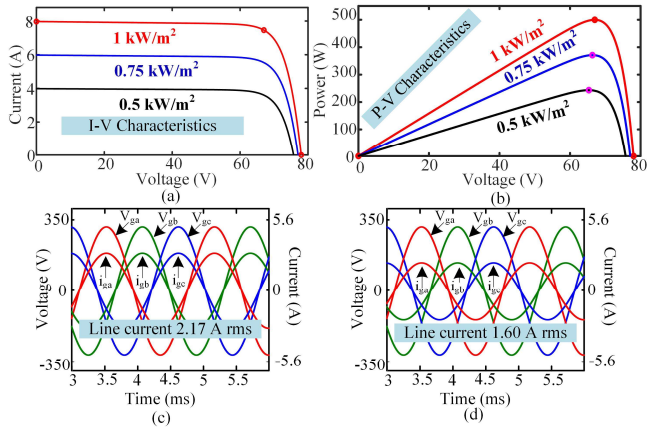

Fig. 9. (a) I-V characteristics of PV for different insolation, (b) P-V characteristics of PV for different insolation, (c) grid voltage and current when all the PV arrays are working at 1 kW/m^2 insolation, and (d) grid voltage and current when three PV arrays are working at 1 kW/m^2, 0.75 kW/m^2 , 0.5 kW/m^2 insolation.

Three PV arrays used in this test utilize separate MPPT with the boost converters. The perturbation and observation method [16] has been used to control the boost converter duty cycle. The main objective of the boost converter is to provide a fixed dc output voltage and also track the maximum power point from the PV. The boost converters are usually employed in PV systems to maintain the desired output voltage, since the output voltage of the PV can be widely varied. Therefore, the boost converter is needed when the PV system has unstable and fluctuating output. If the PV system uses both boost converter and an inverter, the boost converter can enhance the dc output voltage stability, and therefore, reduce the effect of fluctuation on the ac output [17]. The efficiency of the boost converter is also known to be very high [18]. With the use of MOSFET and 500 kHz switching frequency, the boost converter shows more than 97% efficiency [18].

When more power are available at the PV side, then the dc link voltage increases and to maintain the fixed dc link voltage, the dc link voltage regulator increases the reference value of the current (I_d*). Similarly, if the amount of power generation reduces, the dc link voltage decreases and to maintain the fixed dc link voltage, the controller decreases the reference value of the current (I_d*). Therefore, when the PV side has more power, then the inverter injects more current to the grid; and when the PV side has less power, then the inverter injects less current to the grid.

III. Switching Technique for the Proposed Converter

An advance PWM technique for a single phase inverter has been proposed in [19]. The modulation technique can reduce the total harmonic distortion (THD) and the converter loss compared to the traditional switching techniques. This paper investigates an advanced PWM technique suitable for used in a three phase inverter [3]. The advanced third harmonic injected sixty degree bus clamping PWM (THSDBCPWM) is shown in Fig. 10.

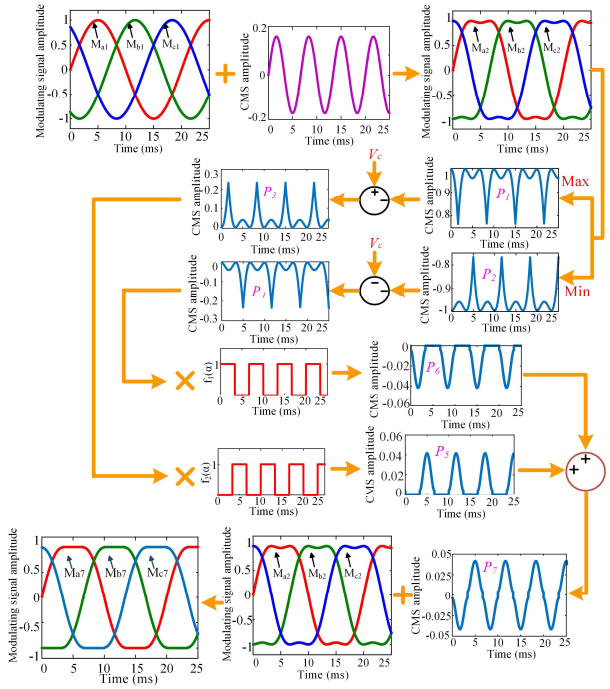

Fig. 10. The operation of the THSDBCPWM for the proposed converter topology.

At first, a third harmonic signal has been added with the sinusoidal PWM (SPPWM) signal and the third harmonic injected PWM (THPWM) (M_{a2}, M_{b2} & M_{c2}) signal is formed. After that, the common mode signals, P_1 & P_2, are formed which are the maximum and the minimum values of the third harmonic injected signal with respect to time. In the next step, the P_1 signal is subtracted from the peak value of the carrier signal (V_c) and then the P_3 signal is formed. Similarly, the P_2 signal is subtracted from the negative peak of the carrier signal ($-V_c$) and the P_4 signal is formed. Then, the P_3 signal is multiplied with $f_2(\alpha)$ and the P_4 signal is multiplied with $f_1(\alpha)$ and the P_5 and the P_6 signals are formed respectively.

The addition of the P_5 and the P_6 signals forms the P_7 CMS. Eventually, the P_7 signal is added with the THPWM to form the THSDBCPWM. Here, $f_1(\alpha)$ and the $f_2(\alpha)$ are the periodic function of α and defined as:

$$f_1(\alpha) = 0 \quad (when \quad 0^\circ < \alpha < 60^\circ) \\ = 1 \quad (when \quad 60^\circ < \alpha < 120^\circ) \tag{1}$$

$$f_2(\alpha) = 1 \quad (when \quad 0^\circ < \alpha < 60^\circ) \\ = 0 \quad (when \quad 60^\circ < \alpha < 120^\circ) \tag{2}$$

The performance of the other popular PWM techniques such as the sinusoidal PWM (SPPWM), the THPWM, conventional space vector PWM (CSVPWM), the trapezoidal PWM (TRPWM), the sixty degree bus clamping PWM (SDBCPWM), the thirty degree bus clamping PWM (TDBCPWM) and the third harmonic injected thirty degree bus clamping PWM (THTDBCPWM) is also investigated for the proposed power converter topology. The mathematical expression of these switching techniques is presented in Table III.

TABLE III
DIFFERENT SWITCHING TECHNIQUE WITH MATHEMATICAL EXPRESSION

PWM	Mathematical expression
SPPWM	$M_1 = A\sin(\omega t+\theta)$ $[M_{a1} \quad M_{b1} \quad M_{c1}] = [M_{1_{\theta=0^\circ}} \quad M_{1_{\theta=120^\circ}} \quad M_{1_{\theta=240^\circ}}]$
THPWM	$C = kA\sin(3\omega t)$ $M_2 = A\sin(\omega t+\theta)+C$ $[M_{a2} \quad M_{b2} \quad M_{c2}] = [M_{2_{\theta=0^\circ}} \quad M_{2_{\theta=120^\circ}} \quad M_{2_{\theta=240^\circ}}]$
CSVPWM	$M_3 = \frac{2}{\sqrt{3}}\left[A\sin(\omega t+\theta) - \frac{1}{2}\{\max(M_{a1},M_{b1},M_{c1}) + \min(M_{a1},M_{b1},M_{c1})\}\right]$ $[M_{a3} \quad M_{b3} \quad M_{c3}] = [M_{3_{\theta=0^\circ}} \quad M_{3_{\theta=120^\circ}} \quad M_{3_{\theta=240^\circ}}]$
TRPWM	$M_4 = A\sin^{-1}\{\sin(\omega t+\theta)\}$ $= 0.98A \quad (when\ M_4 > 0.98A)$ $= -0.98A \quad (when\ M_4 > 0.98A)$ $[M_{a4} \quad M_{b4} \quad M_{c4}] = [M_{4_{\theta=0^\circ}} \quad M_{4_{\theta=120^\circ}} \quad M_{4_{\theta=240^\circ}}]$
SDBCPWM	$M_5 = A\sin(\omega t+\theta) + f_2(\alpha)\{V_c - \max(M_{a1},M_{b1},M_{c1})\} + f_1(\alpha)\{-V_c - \min(M_{a1},M_{b1},M_{c1})\}$ $[M_{a5} \quad M_{b5} \quad M_{c5}] = [M_{5_{\theta=0^\circ}} \quad M_{5_{\theta=120^\circ}} \quad M_{5_{\theta=240^\circ}}]$
TDBCPWM	$M_6 = A\sin(\omega t+\theta) + f_1(\alpha)\{V_c - \max(M_{a1},M_{b1},M_{c1})\} + f_2(\alpha)\{-V_c - \min(M_{a1},M_{b1},M_{c1})\}$ $[M_{a6} \quad M_{b6} \quad M_{c6}] = [M_{6_{\theta=0^\circ}} \quad M_{6_{\theta=120^\circ}} \quad M_{6_{\theta=240^\circ}}]$
THSDBCPWM	$M_7 = A\sin(\omega t+\theta) + f_2(\alpha)\{V_c - \max(M_{a2},M_{b2},M_{c2})\} + f_1(\alpha)\{-V_c - \min(M_{a2},M_{b2},M_{c2})\} + C$ $[M_{a7} \quad M_{b7} \quad M_{c7}] = [M_{7_{\theta=0^\circ}} \quad M_{7_{\theta=120^\circ}} \quad M_{7_{\theta=240^\circ}}]$
THTDBCPWM	$M_8 = A\sin(\omega t+\theta) + f_1(\alpha)\{V_c - \max(M_{a2},M_{b2},M_{c2})\} + f_2(\alpha)\{-V_c - \min(M_{a2},M_{b2},M_{c2})\} + C$ $[M_{a8} \quad M_{b8} \quad M_{c8}] = [M_{8_{\theta=0^\circ}} \quad M_{8_{\theta=120^\circ}} \quad M_{8_{\theta=240^\circ}}]$

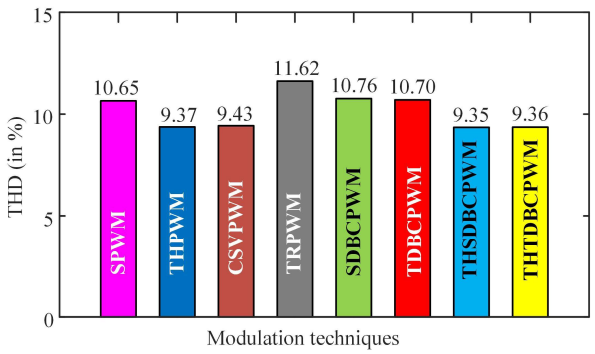

Fig. 11. The performance of different switching techniques in terms of the total harmonic distortion for the proposed converter topology (with a 1 kHz carrier frequency).

Fig. 11 shows the performance of the different modulation techniques in terms of the total harmonic distortion for the proposed converter topology. The THSDBCPWM shows the lowest THD and the TRPWM shows the highest THD among the switching techniques. Fig. 12 shows the surface plot of the THD in the line voltages for the THSDBCPWM with variations of the frequency and the modulation index. The lowest THD is obtained at 1 kHz and modulation index of 1.

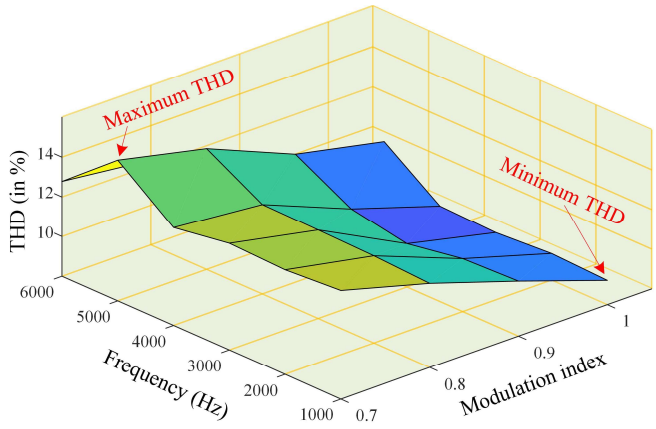

Fig. 12. The surface plot of the THD in the line voltage for the THSDBCPWM.

IV. LOSS ANALYSIS OF THE PROPOSED CONVERTER TOPOLOGY

The inverter total loss can be classified into two parts, the switching loss and the conduction loss. The bipolar junction transistor is just a single switch, whereas, the insulated gate bipolar transistor (IGBT) consists of a switch and an anti-parallel diode. The total conduction loss (P_{cl}) is the summation of the switch and the diode conduction loss and can be expressed as (3)

$$P_{cl} = \frac{1}{2\pi}\left[\int_0^{2\pi}[v_{ce}(t)\ i_c(t)]\ d(wt) + \int_0^{2\pi}[v_F(t)\ i_F(t)]\ d(wt)\right] \quad (3)$$

where $V_{ce}(t)$, $i_c(t)$,$v_F(t)$ and $i_F(t)$ are the instantaneous voltage across the switch, the instantaneous current through the switch, the instantaneous voltage across the diode and the instantaneous current through the diode respectively. For N switches, the total conduction loss (P_{CL}) can be expressed as follows.

$$P_{CL} = \sum_{j=1}^{N} P_{cl_j} \quad (4)$$

For switching loss analysis, the losses can be expressed as a function of the switch current from the corresponding switch datasheet [5]. The total switching loss (P_{SL}) can be expressed as follows.

$$P_{SL} = \frac{1}{T_0}\left[\sum_{j=1}^{N} E_{on_j}(i_c) + \sum_{j=1}^{N} E_{off_j}(i_c) + \sum_{j=1}^{N} E_{rec_j}(i_F)\right] \quad (5)$$

where E_{on}, E_{off} and E_{rec} are the switch turn on, the switch turn off and the diode turn off energy in joule. Therefore, the total inverter loss (P_{TL}) can be expressed as follows.

$$P_{TL} = P_{CL} + P_{SL} \tag{6}$$

Fig. 13 shows the different losses for the different PWM techniques with the proposed power converter topology. The THSDBCPWM shows the lowest and the THPWM shows the highest total inverter loss among the PWM techniques.

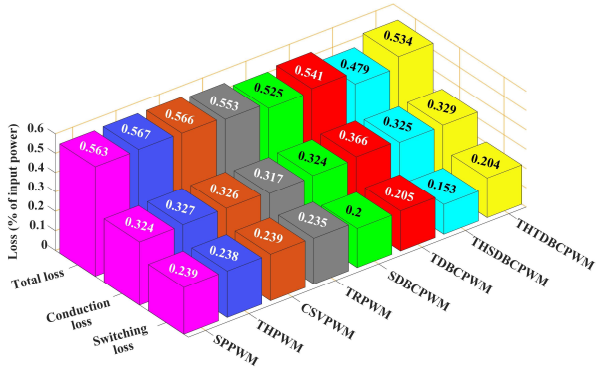

Fig. 13. The inverter loss analysis for different modulation techniques.

Fig. 14 shows the loss distribution among the switches for the proposed power converter topology. The S_8 switch shows the lowest and the S_7 switch shows the highest switching loss among the 10 switches. Moreover, the S_9 and the S_{10} switches show the lowest and the S_1 switch shows the highest conduction loss among the switches. In case of the total loss, the S_8 switch shows the lowest and the S_7 shows the highest loss among the switches. This loss distribution analysis is done to design the heat sinks for the electronic switches.

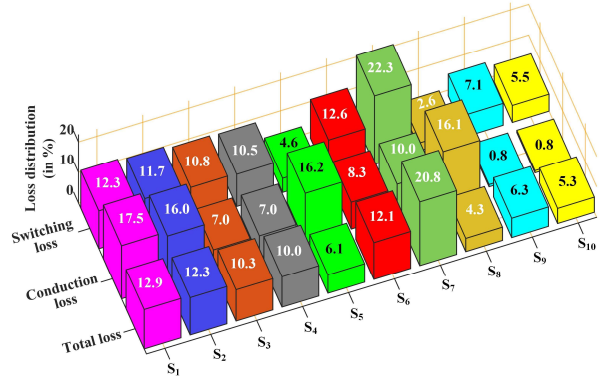

Fig. 14. The loss distribution among the switches for the proposed power converter.

V. Experimental Validation of The Proposed Converter Topology

Fig. 15(a) shows the experimental setup to validate the proposed power converter topology. A reduced scale test platform has been developed for the validation of the proposed power converter topology. The 43 A, 1200 V, HGTG11N120CND IGBT and the 15 A, 350 V, MJL4281A npn bipolar transistor have been considered as the switching devices to develop the prototype of the 7-level power converter in the laboratory. The dSPACE MicroLabBox and the ACPL-P343 driver circuit are used to implement the THSDBCPWM switching algorithm of the proposed converter. The AMATEK TerraSAS PV simulator ETS 1000/10 (acting as the photovoltaic array) is connected with the California Instruments MX45 programmable power supply (acting as the supply grid) through the developed power converter. Fig. 15(b) shows the developed ANPC separately, the dimension of which is around 100 mm * 80 mm.

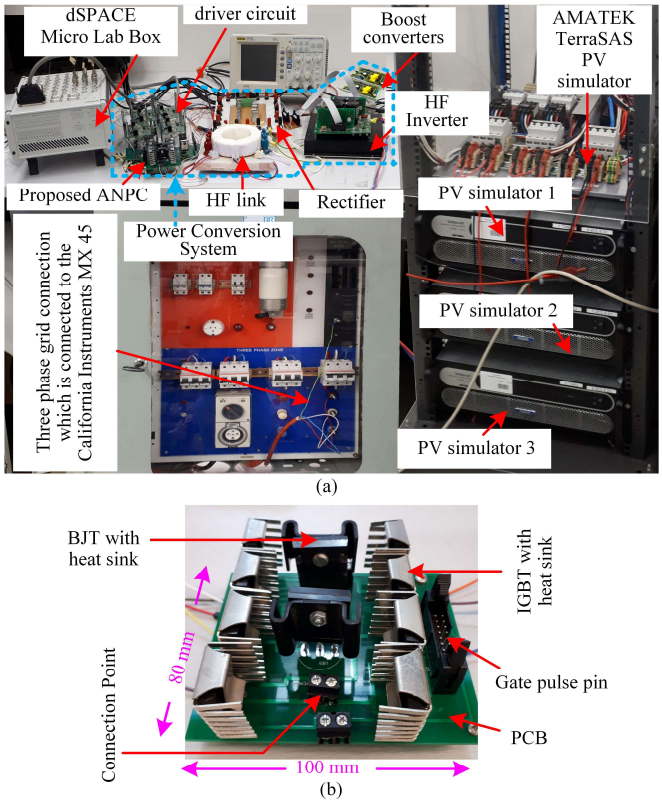

Fig. 15. (a) Experimental setup for the validation of the proposed converter with the high frequency (HF) magnetic link and (b) proposed ANPC.

Fig. 16(a)–16(c) show three different real-life irradiance and temperature profiles (case 1, case 2 and case 3) that are fed into the solar emulator. Here, the green line indicates the current operating point for the PV emulator. For Fig. 16 (a)–16(c) the operating point is around 1000 W/m^2, 200 W/m^2 and 250 W/m^2, respectively. Fig. 16(d)–16(f) show the I-V and P-V characteristics for different operating points on the irradiance profiles. Therefore, Fig. 16 (d) show the I-V and P-V characteristics when the PV array gets irradiance of 1000 W/m^2. Similarly, Fig. 16 (e) and 16 (f) are self-explanatory. Fig. 16(g)–16(i) show the PV output voltage and current for case 1, case 2 and case 3, respectively. Here, the PV arrays provide different voltage and current due to the irradiance, temperature, I-V characteristics and maximum power point tracking. Fig. 16(j) show the dc bus voltage for the both situations, situation 1: when all the PV array follow case 1 and situation 2: when three PV array follow case 1, case 2 and case 3, respectively. Thus, the boost converters always maintain the dc bus voltage fixed.

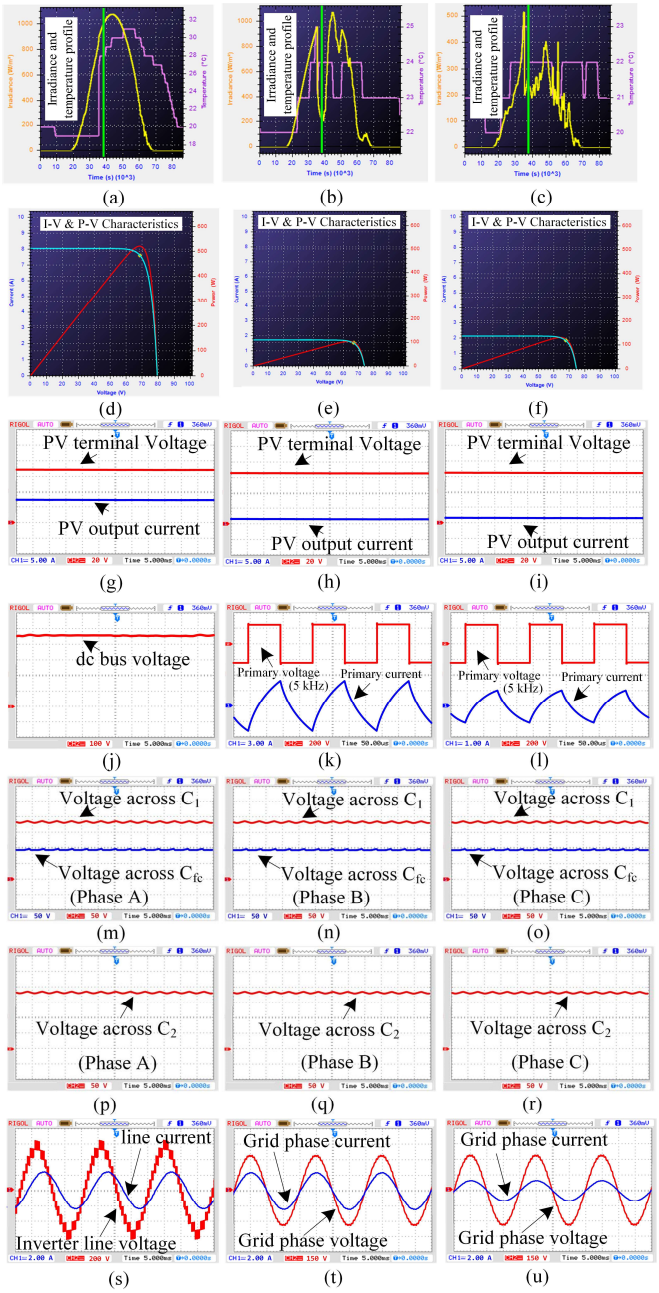

Fig. 16. (a) Solar irradiance and temperature profile case 1, (b) solar irradiance and temperature profile case 2, (c) solar irradiance and temperature profile case 3, (d) I-V and P-V characteristics for case 1, (e) I-V and P-V characteristics for case 2, (f) I-V and P-V characteristics for case 3, (g) PV array output voltage and current for case 1, (h) PV array output voltage and current for case 2, (i) PV array output voltage and current for case 3, (j) dc bus voltage for situation 1 and 2, (k) primary voltage and current of HF magnetic link when all PV arrays follow case 1, (l) primary voltage and current of HF magnetic link when three PV arrays follow case 1, case 2 and case 3, respectively, (m) voltages across C_1 and C_{fc} capacitor for phase A, (n) voltages across C_1 and C_{fc} capacitor for phase B, (o) voltages across C_1 and C_{fc} capacitor for phase C, (p) voltage across the C_2 capacitor for phase A, (q) voltage across the C_2 capacitor for phase B, (r) voltage across the C_2 capacitor for phase C, (s) inverter output line voltage and line current under situation 1, (t) grid voltage and current under situation 1, and (u) grid voltage and current under situation 2.

Fig. 16 (k) show the high frequency magnetic link primary voltage and current when all the PV arrays follow case 1 and Fig. 16 (l) show the high frequency magnetic link primary voltage and current when three PV arrays follow case 1, case 2 and case 3, respectively. Here, the primary voltage is identical in both cases but the primary current is different. When all the PV arrays get high irradiance then the primary current is high and when the PV arrays get low irradiance then the primary current is low. Fig. 16 (m)–16(r) show the capacitor voltage waveforms for the both situations, situation 1: when all the PV array follow case 1 and situation 2: when three PV array follow case 1, case 2 and case 3, respectively. Here, three different currents from the PV arrays are added together and fed into the magnetic link. The primary current creates the magnetic flux and the same flux cuts all the secondary windings. Therefore, the capacitor voltages show identical shapes. Fig. 16(s) shows the inverter line voltage and current under situation 1. Fig. 16 (t) shows grid voltage and current under situation 1 and Fig. 16 (u) shows the grid voltage and current under situation 2.

The output voltage and current from the solar emulator are the inputs into the system and the grid voltage and injected current to the grid are the outputs of the system. The data from Fig. 16(g)–16(i) and Fig. 16(u) are collected in CSV format and used in MATLAB. Three solar emulator voltages and currents are multiplied and added together to measure the input power. Also, the grid rms voltage and the injected rms current are multiplied and the output power is measured. By dividing the input power by the output power, the system efficiency is found to be 80%. However, considering the ANPC inverter input power instead of the PV array power, the ANPC inverter efficiency is found to be 96% which is close to the theoretical analysis. In the traditional systems, the use of the power frequency step up transformers and the filter circuits increases the total loss by 50% and the system volume by 40% [20]. The power conversion system efficiency and the proposed inverter efficiency is also comparable to the traditional magnetic linked multilevel inverters, where for 100% loading, the system and the converter efficiency were found to be 76% and 95% respectively [21].

The inverter output line voltage (before the line filter) and the grid phase voltage are also collected in CSV format and in MATLAB environment the frequency spectrums are analyzed (as shown in Fig. 17(a) and Fig. 17(b)).

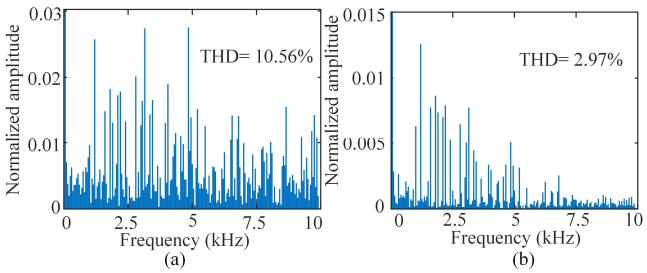

Fig. 17. (a) Inverter line voltage frequency spectrum and (b) grid phase voltage frequency spectrum.

To observe the dynamic response of the inverter a fast-changing irradiance profile with constant temperature has been fed into the three PV emulators. Fig. 18 (a) and 18 (c) show the irradiance profile with constant temperature of 25° C.

From 0 to 30 seconds the irradiance is 100 W/m^2, from 31 to 65 seconds the irradiance is 800 W/m^2 and from 66 to 95 seconds the irradiance is again 100 W/m^2. Fig. 18 (b) shows the I-V and P-V characteristics when the operating point is on 100 W/m^2 irradiance and Fig. 18 (d) shows the I-V and P-V characteristics when the operating point is on 800 W/m^2 irradiance.

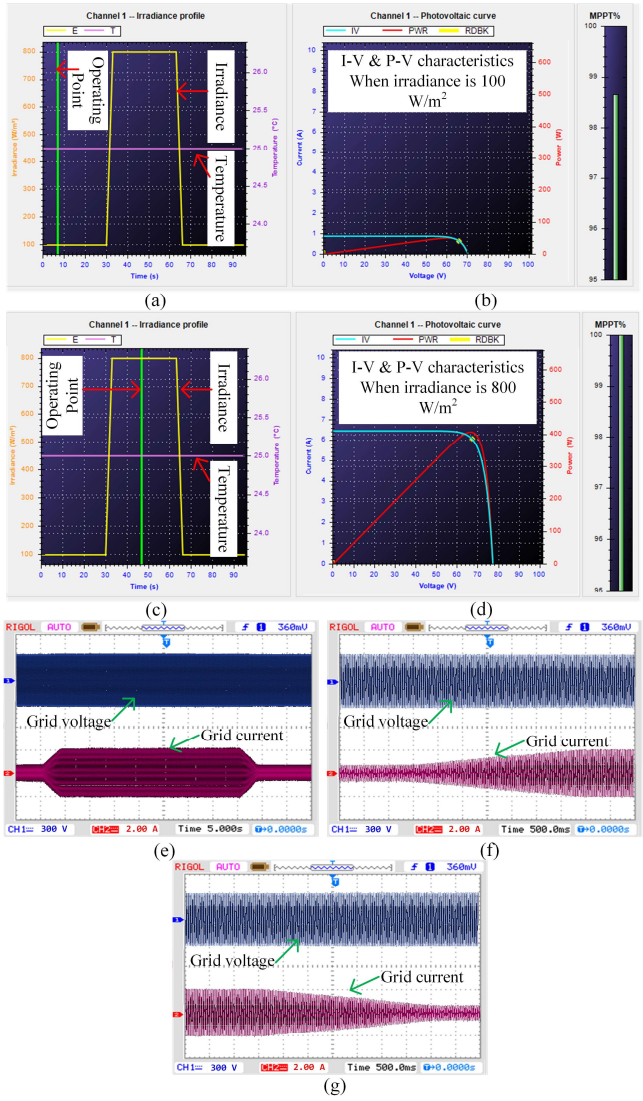

Fig. 18 (a) PV irradiance and temperature profile when the operating point is on 100 W/m^2, (b) I-V and P-V characteristics when the operating point is on 100 W/m^2, (c) PV irradiance and temperature profile when the operating point is on 800 W/m^2, (d) I-V and P-V characteristics when the operating point is on 800 W/m^2, (e) grid voltage and current, (f) zoomed version of grid voltage and current when the irradiance changes from 100 W/m^2 to 800 W/m^2, and (g) zoomed version of grid voltage and current when the irradiance changes from 800 W/m^2 to 100 W/m^2.

Fig. 18 (e) shows the grid voltage and current for the whole scenario. Fig. 18 (f) shows the zoomed version of grid voltage and current when the irradiance changes from 100 W/m^2 to 800 W/m^2 and Fig. 18 (g) shows the zoomed version of grid voltage and current when the irradiance changes from 800 W/m^2 to 100 W/m^2. From the grid voltage and current waveforms, it can be seen that the grid voltage is always identical but the current changes according to the available power from the PV side. When the irradiance changes from 100 W/m^2 to 800 W/m^2 the current reaches around three times of the initial current.

VI. Comparative Assessment of The Proposed Converter Topology

The comparison of the proposed converter topology with the other popular power converters in terms of the number of components is presented in Table V.

TABLE V
COMPARISON OF THE PROPOSED TOPOLOGY WITH OTHER POPULAR 7-LEVEL SINGLE PHASE CONVERTERS IN TERMS OF NUMBER OF COMPONENTS

Converters	Number of			
	Sources	IGBTs	Capacitors	Diodes
Cascaded H-bridge[6]	3	12	-	-
Diode clamped [6]	1	12	6	10
Capacitor clamped [6]	1	12	7	-
Conventional ANPC [12]	1	10	4	-
ANPC Proposed in [22]	1	14	7	1
Proposed ANPC	1	10	3	-

The use of the capacitors makes the system bulky and less reliable. Although the proposed converter topology requires the same number of electronic switches as the conventional ANPC converter, it requires less number of flying capacitors than the traditional ones. Thus proposed topology reduces the size of the converter and increases the reliability of the power conversion system.

Table VI show the performance metrics of different 7-level power converters.

TABLE VI
PERFORMANCE METRICS OF DIFFERENT 7-LEVEL SINGLE PHASE CONVERTERS

Converters	Performance indicators			
	Effective dc bus utilization	Simple control	Voltage balancing problem	Reduced converter size
Cascaded H-bridge[6]	√	√	√	×
Neutral point clamped [6]	×	×	√	×
Capacitor clamped [6]	×	×	√	×
Conventional ANPC [12]	×	×	√	×
ANPC Proposed in [22]	×	×	√	×
Proposed ANPC	√	√	×	√

The proposed power converter topology utilizes the input dc bus voltage better than the traditional ANPC power converter. Moreover, no additional control technique is required to keep the voltages across the three flying capacitors balanced. The high frequency magnetic link generates isolate and balanced multiple sources and maintains the voltages across the three flying capacitors balanced. Here, all the available powers from the PV side are converted into magnetic energy and the same magnetic flux cuts the secondary windings. Therefore, all the single phase units of the proposed inverter get the same input voltage and the voltage balancing at the grid side is ensured. Thus the proposed topology prevents the three phase system from being unbalanced. The proposed power converter topology also provides galvanic isolation with a single core manufactured with advanced material. The lack of galvanic isolation is a big issue faced by

the traditional power frequency transformer-less grid connected PV systems. The proposed topology eliminates the use of power frequency transformer and also reduces the size of the filter circuit. Thus, the proposed converter topology can make the grid connected PV system more compact and more efficient.

VII. Conclusion

This paper proposes a magnetic linked multilevel active neutral point clamp converter with an advanced switching technique for the grid integration of the PV systems. The proposed converter topology uses less number of capacitors and makes the power conversion system compact and reliable. The proposed power converter utilizes the input dc bus voltage better than the traditional ANPC converters. The proposed power converter eliminates the voltage balancing problems and makes the control strategy simple. The proposed converter also provides galvanic isolation to the grid connected PV systems. The advanced switching technique ensures less harmonic distortion and less converter loss. Thus, the proposed power converter with the advanced switching technique can make the grid connected PV system more compact, more reliable and more efficient.

VIII. Acknowledgement

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